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EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2133	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/976,701	DORSEY, MICHAEL C.	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☒ Claim(s) *1,8,15,16,23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-39 are presented for examination.

Information Disclosure Statement

The examiner has considered the applicants Information Disclosure Statement.

Drawings

1. The drawings are objected to because The drawings are objected to because:

   a. FIG.2 LSSD and STEP CLKS are not referred to in the disclosure.

   b. FIG.9 LSSD_CLKA, LSSD_CLKB, LBST_SCAN_CLKA and LBST_SDCAN_CLKB are not referred to in the disclosure.

   c. FIG.1 195 is referred to in the disclosure as 195a-d.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

   a. Page 5 line 19 recites "synchronous random access memory ("SRAMs")". The statement is a combination of two terms; "Static Random Access Memory, an SRAM", and "Synchronous Dynamic Random Access Memory, an SDRAM", the terms of which are generally accepted in the

art. The examiner suspects that the applicant wishes to recite a "static random access memory", but would like the applicant to respond as to the device type specifically intended. Appropriate correction is required.

b. The disclosure is objected to because of the following informalities: page 7 line 2 describes engine 110 being configured by a 66 bit signal composed of a 32 bit vector and 33 bit seed. The sum of 32 and 33 is not 66. Appropriate correction is required.

c. The disclosure is objected to because of the following informalities: page 9 line 15 recites, "31", but the examiner believes that it should read, "32". Appropriate correction is required.

d. The disclosure is objected to because of the following informalities: page 9 line 28 recites, "LBST_STEP_STEPE", but the examiner cannot find this reference in FIG.9. Appropriate correction is required.

e. The disclosure is objected to because of the following informalities: page 10 line 2 recites, "components 150", but the examiner cannot find this reference in the drawings. Appropriate correction is required.

f. The disclosure is objected to because of the following informalities: page 11 line 10, page 13 lines 20 and 22 recite, "ASIC 100", but the examiner cannot find this reference in the drawings, and believes it should read "ASIC 150". Appropriate correction is required.

g. The disclosure is objected to because of the following informalities: page 12 line 23 recites, "initialized them to...", but the examiner believes it

should read "initialized to...". Appropriate correction is required.

Claim Objections

3. Claims 1, 8, 15, 16 and 23 are objected to because of the following informalities: each claim contains the term "capable of", which is not a positive limitation. Appropriate correction is required.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 15, 16, 17, 19, 21 and 22 are provisionally rejected under the judicially created doctrine of double patenting over claims 11, 13, 14, 15, 16, 17 and 18 of copending Application No. 09/976707. This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending

application since the referenced copending application and the instant application are claiming common subject matter, as follows:

15. A integrated circuit device including: a plurality of memory components; a testing interface; and a built-in self-test controller controlled through the testing interface, the built-in self-test controller including: a memory built-in self-test engine capable of performing a memory built-in self-test; and a memory built-in self-test signature generated upon an execution of the memory built-in self-test.

16. The integrated circuit device of claim 15, wherein the memory built-in self-test signature register is further capable of storing the results of at least one paranoid check.

17. The integrated circuit device of claim 15, wherein the memory built-in self-test signature register includes a bit indicating whether the memory built-in self-test is done.

19. The integrated circuit device of claim 15, wherein the memory built-in self-test state machine comprises: a reset state entered upon receipt of an external reset signal; an initiate state entered from the reset state upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal; a flush state entered from the initiate state upon the initialization of components and signals in the memory built-in self-test domain in the initiate state; a test state entered into from the flush state; and a done state entered into upon completing the test of each of a plurality of memory components in the memory built-in self-test.

21. The integrated circuit device of claim 15, wherein the memory components include a static random access memory device.

22. The integrated circuit device of claim 15, wherein the testing interface comprises a Joint Test Action Group tap controller.

Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Also, a later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because

the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 2, 10, 16, 28 and 36 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claims specify using a "paranoid check" for a purpose within a MBIST signature register. The same term is mentioned in the disclosure but the term was never defined. The examiner, being one with ordinary skill in the art, is unsure of what the applicant means when using this term.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 2, 10, 16, 28 and 36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "paranoid check" in claims 2, 10, 16, 28 and 36 is used in the claims and refers to a test which the examiner is not familiar. While the examiner believes the phrase to mean "to check again by some other means.", the term is indefinite because the specification does not clearly redefine the term.

7. Claim 5 recites the limitation "the memory built-in self-test domain" in line 7 of the claim. There is insufficient antecedent basis for this limitation in the claim.

8. Claim 7 recites the limitation "the memory built-in self-test engines" in line 1, and "the memory built-in self-test domain" in line 7 of the claim. There is insufficient antecedent basis for this limitation in the claim.

9. Claim 19 recites the limitation "the memory built-in self-test machine" in line 1, and "the memory built-in self-test domain" in line 7 of the claim. There is insufficient antecedent basis for this limitation in the claim.

10. Claim 32 recites the limitation "the contents of the memory components" in line 1 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1, 2, 4, 6, 8, 9, 10, 12, 13, 14, 15, 16, 18, 20 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Motika et al., U.S. Patent No. 5982189.

As per Claim 1:

Motika et al. teaches a built-in self-test controller (FIG.2 32, 36) including: a memory built-in self-test engine capable of executing a memory built-in self-test (FIG.2 50 and 32); and a memory built-in self-test signature generated on execution of the memory built-in self-test (column 3 lines 50-63).

As per Claim 2:

Motika et al. teaches the built-in self-test controller of claim 1, wherein the memory built-in self-test signature register includes the results of at least one paranoid check (column 3 lines 50-63). Note: the examiner is unsure of the meaning of "paranoid check" (see 112 rejections above).

As per Claim 4:

Motika et al. teaches the built-in self-test controller of claim 1, wherein the memory built-in self-test engine comprises: a memory built-in self-test state machine

(FIG.2 32); and a nested memory built-in self-test engine (FIG.2 50) operating the memory built-in self-test state machine.

As per Claim 6:

Motika et al. teaches the built-in self-test controller of claim 1 (FIG.2 32, 36), wherein the memory built-in self-test engine (FIG.2 50 and 32) comprises: a plurality of alternative memory built-in self-test state machines (FIG.2 32); and a nested memory built-in self-test engine (FIG.2 50) operating a predetermined one of the memory built-in self-test state machines (column 4 lines 6-54).

As per Claim 8:

Motika et al. teaches the built-in self-test controller of claim 1, further comprising: a logic built-in self-test engine (FIG.2 50 and 34) capable of executing a logic built-in self-test (FIG.2 34, 38) and storing the results thereof (column 3 lines 38-67 and column 4 lines 1-5); and a multiple input signature register capable of storing the results of an executed logic built-in self-test (column 3 lines 56-60).

As per Claim 9:

Motika et al. teaches a built-in self-test controller (FIG.2 50, 32) including: means for executing a memory built-in self-test (FIG.2 50, 32, 36); and means for storing the results generated on execution of the memory executing means (column 3 lines 38-63).

As per Claim 10:

Motika et al. teaches the built-in self-test controller of claim 9, wherein the memory storing means includes the results of at least one paranoid check (column 3

lines 50-63). Note: the examiner is unsure of the meaning of "paranoid check" (see 112 rejections above).

As per Claim 12:

Motika et al. teaches the built-in self-test controller of claim 9 (FIG.2 50, 32), wherein the memory executing means comprises: a memory built-in self-test state machine (FIG.2 32); and a nested memory built-in self-test engine (FIG.2 50) operating the memory built-in self-test state machine (column 4 lines 6-54).

As per Claim 13:

Motika et al. teaches the built-in self-test controller of claim 9 (FIG.2 50, 32), wherein the memory executing means comprises: a plurality of alternative memory built-in self-test state machines (FIG.2 32); and a nested memory built-in self-test engine (FIG.2 50) operating a predetermined one of the memory built-in self-test state machines (column 4 lines 6-54).

As per Claim 14:

Motika et al. teaches the built-in self-test controller of claim 9 (FIG.2 50, 32), further comprising: means for executing a logic built-in self-test (FIG.2 34, 38) and storing the results thereof; and means for storing the results of an executed logic built-in self-test (column 3 lines 38-67 and column 4 lines 1-5).

As per Claim 15:

Motika et al. teaches a integrated circuit device (column 1 lines 5-8) including: a plurality of memory components (FIG.2 36); a testing interface (FIG.2 60); and a built-in self-test controller (FIG.2 50) controlled through the testing interface (column 4 lines 44-

47), the built-in self-test controller including: a memory built-in self-test engine (FIG.2 50) capable of performing a memory built-in self-test (column 4 lines 6-7); and a memory built-in self-test signature generated upon an execution of the memory built-in self-test (column 3 lines 38-63).

As per Claim 16:

Motika et al. teaches the integrated circuit device of claim 15, wherein the memory built-in self-test signature register is further capable of storing the results of at least one paranoid check (column 3 lines 50-63). Note: the examiner is unsure of the meaning of "paranoid check" (see 112 rejections above).

As per Claim 18:

Motika et al. teaches the integrated circuit device of claim 15 (FIG.2 60, 50, 36), wherein the memory executing means comprises: a memory built-in self-test state machine (FIG.2 32); and a nested memory built-in self-test engine (FIG.2 50) operating the memory built-in self-test state machine (column 4 lines 6-54).

As per Claim 20:

Motika et al. teaches the integrated circuit device of claim 15 (FIG.2 60, 50, 36), wherein the memory executing means comprises: a plurality of alternative memory built-in self-test state machines (FIG.2 32); and a nested memory built-in self-test engine (FIG.2 50) operating a predetermined one of the memory built-in self-test state machines (column 4 lines 6-54).

As per Claim 23:

Motika et al. teaches the integrated circuit device of claim 15 (FIG.2 36, 50, 60) further comprising: a logic built-in self-test engine capable of executing a logic built-in self-test (FIG.2 32) and storing the results thereof (column 3 lines 38-63); and a multiple input signature register capable of storing the results of an executed logic built-in self-test (column 3 lines 56-60).

12. Claims 24-28, 30 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Lo et al., U.S. Patent No. 5661732.

As per Claim 24:

Lo et al. teaches a method for performing a memory built-in self-test (column 4 line 52), the method comprising: externally resetting a memory built-in self-test engine (column 5 line 7) and a memory built-in self-test signature (column 7 lines 54-57); generating the memory built-in self-test signature upon an execution of a memory built-in self-test by the memory built-in self-test engine (column 12 line 8); and reading the generated memory built-in self-test signature (column 7 lines 65-67 and column 8 lines 1-6).

As per Claim 25:

Lo et al. teaches the method of claim 24, wherein the execution of the memory built-in self-test includes: initiating a plurality of components and signals in a memory built-in self-test engine (column 6 lines 31-35) and the memory built-in self-test signature (column 7 lines 56-61) upon receipt of at least one of a memory built-in self-test run signal (column 5 line 7) and a memory built-in self-test select signal; flushing the contents of a plurality of memory components to a known state after initialization of

the components and the signals (column 13 lines 7-9); and testing the flushed memory components (same reference).

As per Claim 26:

Lo et al. teaches the method of claim 25, wherein generating the memory built-in self-test signature includes: storing the results of the testing in a memory built-in self-test signature register (column 8 lines 4-6).

As per Claim 27:

Lo et al. teaches the method of claim 24, wherein generating the memory built-in self-test signature includes storing the results of the testing in a memory built-in self-testing register (column 4 lines 21-25).

As per Claim 28:

Lo et al. teaches the method of claim 24, wherein performing the memory built-in self-test further includes at least one of: performing at least one paranoid check; and storing the results of the paranoid check in the memory built-in self-test signature register (column 4 lines 21-25). Note: the examiner is unsure of the meaning of "paranoid check" (see 112 rejections above).

As per Claim 30:

Lo et al. teaches the method of claim 24, wherein externally resetting the memory built-in self-test engine (column 5 line 7) includes externally resetting a memory built-in self-test engine including: a memory built-in self-test state machine; and a nested memory built-in self-test engine (column 6 lines 31-46 and column 7 lines 1-61).

As per Claim 32:

Lo et al. teaches the method of claim 30, wherein flushing the contents of the memory components includes flushing the contents of a plurality of static random access memories (column 16 lines 21-25 and column 2 line 18).

13. Claims 33-36 and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Kraus et al., U.S. Patent No. 6587979.

As per Claim 33:

Kraus et al. teaches a method for performing a built-in self-test on an integrated circuit device (column 1 lines 12-17), the method comprising: interfacing the integrated circuit device with a tester (FIG.5 21); performing a memory built-in self-test (column 2 lines 43-46), including: externally resetting a memory built-in self-test engine (FIG.6 24 is RESET from JTAG 55) and a memory built-in self-test signature (FIG.6 54); generating the memory built-in self-test signature upon an execution of a memory built-in self-test by the memory built-in self-test engine (FIG.6 SET for 54); and reading the generated memory built-in self-test signature (FIG.6 FAIL).

As per Claim 34:

Kraus et al. teaches the method of claim 33, wherein the execution of the memory built-in self-test includes: initiating a plurality of components and signals in a memory built-in self-test engine (column 13 lines 1-11) and the memory built-in self-test signature register (FIG.6 54) upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal (column 13 line 1); flushing the contents of a plurality of memory components to a known state after initialization of the

components and the signals in the memory built-in self-test domain (column 12 lines 11-27); and testing the flushed memory components (column 12 lines 11-27).

As per Claim 35:

Kraus et al. teaches the method of claim 33, wherein generating the memory built-in self-test signature includes storing the results in a memory built-in self-test signature register (column 12 lines 22-24).

As per Claim 36:

Kraus et al. teaches the method of claim 33, wherein performing the memory built-in self-test further includes at least one of: performing at least one paranoid check; and storing the results of the paranoid check in the memory built-in self-test signature register (column 12 lines 22-24). Note: the examiner is unsure of the meaning of "paranoid check" (see 112 rejections above).

As per Claim 38:

Kraus et al. teaches the method of claim 33, wherein externally resetting the memory built-in self-test engine includes externally resetting a memory built-in self-test engine including: a memory built-in self-test state machine (FIG.16 100); and a nested memory built-in self-test engine (FIG.16 102).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

14. Claims 3, 11, 17 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, and in view of Au et al., U.S. Patent No. 6681359.

As per Claims 3, 11, and 17:

Motika et al. fails to further teach the built-in self-test controller of claims 1, 10 and 15, wherein the memory built-in self-test signature includes a bit indicating whether the memory built-in self-test is done. But, Au et al., in column 9 line 25-33 defines such a feature. It would have been obvious to apply this capability taught by Au et al. to the Motika et al. test system in order to improve pattern handling during test. And Au et al., in column 2 lines 18-27 in reciting the attributes of the invention, boasts of a better means to retrieve information within an MBIST while not requiring a large number of device pins. One with ordinary skill in the art at the time of the invention, motivated by Au et al., would combine the two references, thus the claims are rejected.

As per Claim 22:

Motika et al. fails to further teach the integrated circuit device of claim 15, wherein the testing interface comprises a Joint Test Action Group tap controller. In an analogous art, Au et al. does teach this feature. It would have been obvious to modify the test control interface of Motika et al. to include additional capabilities, such as JTAG, so as not to burden the circuit with extra I/O pins. And Au et al., in column 2 lines 18-27 in reciting the attributes of the invention, boasts of a better means to retrieve information within an MBIST while not requiring a large number of device pins. One with ordinary skill in the art at the time of the invention, motivated by Au et al., would combine the two references, thus the claim is rejected.

15. Claims 5, 7 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, as applied to Claims 4, 6 and 15, and further in view of Zuraski et al., U.S. Patent No. 6560740, Lo et al., U.S. Patent No. 5661732, and Wong et al., U.S. Patent No. 6636997. The LBIST state machine (FIG.2 32) and engine (FIG.2 50, 32) of Motika et al. in Claims 4, 6 and 15 fail to teach a reset sequence in the test entered via an external signal. In an analogous art, Zuraski et al. enters a state via an external reset signal (Zuraski et al, column 10 lines 31-36), an obvious modification in order to control the test circuit during test, but does not begin initializing the device with an LBIST run signal. In another analogous art, Lo et al., enters a 1st state subsequent to a start ABIST signal (Lo et al. column 5 lines 6-8). In order to control operation of the test cycles, it would have been obvious to provide the features of Lo et al. in the same circuit under consideration. And finally, Wong et al. in column 6 lines 26-50 teaches the states of scan, step, and complete (done) as specified

by the applicant's claim. One with ordinary skill would have found it obvious to apply the steps of Wong et al. to the state machine of Lo et al. in performance of an MBIST test which had to scan through each test location. Wong et al., in column 2 lines 62-67, describes an advantage of the invention as being capable of both pseudo-random and functional testing. Lo et al. column 2 lines 38-40 lists an advantage of the invention as being an improvement in test time and test coverage. And Zuraski Jr. et al., professes the advantages (column 2 lines 10-18) of a readily programmable BIST that would not need constant revision as needs change. In view of the motivations for Zuraski et al. and Lo et al., and in view of Wong et al., one with ordinary skill in the art at the time of the invention, would combine all of the references above, thus the claims are rejected.

16. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, as applied to Claim 15 above, in view of Kim et al., U.S. Patent No. 6148426. As per the objection to the disclosure above (paragraph 2a above), the examiner believes that since there does not appear to be a "synchronous random access memory" in the art, the examiner assumes that the applicant wishes to recite "static random access memory" in the subject claims. These claims therefore limit the memory device to being a "static random access memory", which is not taught by Motika et al. But in an analogous art, Kim et al. teaches an MBIST (see Abstract) that is used for testing an SRAM (see Title). It would have been obvious to modify the testing paradigm of Motika et al. to test many differing types of memories, including SRAMs, by applying the teaching of Kim. Citing a savings in BIST size and cost (column 2 lines 55-

61), Kim et al. would motivate one with ordinary skill in the art at the time of the invention to combine the art for the purpose of testing SRAM memories.

17. Claims 29 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al., U.S. Patent No. 5661732, and in view of Au et al., U.S. Patent No. 6681359.

As per Claim 29:

Lo et al. fails to further teach the method of claim 24, wherein performing the memory built-in self-test further includes setting a bit in the memory built-in self-test signature indicating whether the memory built-in self-test is done. But, Au et al., in column 9 line 25-33 defines such a feature. It would have been obvious to apply this capability taught by Au et al. to the Lo et al. test system in order to improve pattern handling during test. And Au et al., in column 2 lines 18-27 in reciting the attributes of the invention, boasts of a better means to retrieve information within an MBIST while not requiring a large number of device pins. One with ordinary skill in the art at the time of the invention, motivated by Au et al., would combine the two references, thus the claims are rejected.

As per Claim 31:

Lo et al. fails to further teach the method of claim 30, wherein externally resetting the memory built-in self-test state machine includes externally resetting one of a plurality of memory built-in self-test state machines. Au et al. however does teach this feature (see FIG. 3 state machines 116). It would have been obvious to apply this capability taught by Au et al. to the Lo et al. test system in order to increase test

capability along with circuit growth. And Au et al., in column 2 lines 18-27 in reciting the attributes of the invention, boasts of a better means to retrieve information within multiple MBISTs while not requiring a large number of device pins. One with ordinary skill in the art at the time of the invention, motivated by Au et al., would combine the two references, thus the claims are rejected.

18. Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus et al., U.S. Patent No. 6587979, and in view of Au et al., U.S. Patent No. 6681359. Kraus et al. fails to teach the method of claim 33, wherein performing the memory built-in self-test further includes setting a bit in the memory built-in self-test signature indicating whether the memory built-in self-test is done. But, Au et al., in column 9 line 25-33 defines such a feature. It would have been obvious to apply this capability taught by Au et al. to the Kraus et al. test system in order to improve pattern handling during test. And Au et al., in column 2 lines 18-27 in reciting the attributes of the invention, boasts of a better means to retrieve information within an MBIST while not requiring a large number of device pins. One with ordinary skill in the art at the time of the invention, motivated by Au et al., would combine the two references, thus the claims are rejected.

19. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus et al., U.S. Patent No. 6587979, and in view of Motika et al., U.S. Patent No. 5982189. Kraus et al. fails to teach the method of claim 33, further comprising: performing a logic built-in self-test; and reading the results of the logic built-in self-test. But Motika et al., in column 3 lines 64-67 and column 4 lines 1-5 does teach this feature. It would have been obvious to modify the system of Kraus et al. to include the teachings of Motika et al. in

order to test further the logic portions of an integrated circuit such as Kraus et al. Motika et al. recites the advantage of testing logic under stress which provide a more reliable circuit (column 1 lines 5-67 and column 2 lines 1-33). One with ordinary skill in the art at the time of the invention, motivated by Motika et al., would combine the two references, thus the claim is rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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